

09/905, 405

Refine Search

Search Results -

Terms	Documents
L10 and (titanium or copper or aluminum)	8

Database:

US Pre-Grant Publication Full-Text Database
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 Derwent World Patents Index
 IBM Technical Disclosure Bulletins

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L11

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DB=USPT; PLUR=YES; OP=ADJ

<u>L11</u>	L10 and (titanium or copper or aluminum)	8	<u>L11</u>
<u>L10</u>	L9 and (polish or polishing)	8	<u>L10</u>
<u>L9</u>	I5 and (dummy near gate)	8	<u>L9</u>
<u>L8</u>	I3 and (dummy near gate)	32	<u>L8</u>
<u>L7</u>	L5 and ((intrametal) near2 (dielectric or IMD))	0	<u>L7</u>
<u>L6</u>	L5 and ((intrametal) adj (dielectric or IMD))	0	<u>L6</u>
<u>L5</u>	L3 and (high adj K)	22	<u>L5</u>
<u>L4</u>	L3 and IMD	4	<u>L4</u>
<u>L3</u>	L2 and (lightly near2 doped)	671	<u>L3</u>
<u>L2</u>	L1 and sidewalls	1201	<u>L2</u>
<u>L1</u>	polysilicon adj gate adj electrodes	2588	<u>L1</u>

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☐ 1. Document ID: US 6353269 B1

L4: Entry 1 of 4

File: USPT

Mar 5, 2002

US-PAT-NO: 6353269

DOCUMENT-IDENTIFIER: US 6353269 B1

TITLE: Method for making cost-effective embedded DRAM structures compatible with logic circuit processing

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KMC	Draw De
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☐ 2. Document ID: US 6265295 B1

L4: Entry 2 of 4

File: USPT

Jul 24, 2001

US-PAT-NO: 6265295

DOCUMENT-IDENTIFIER: US 6265295 B1

TITLE: Method of preventing tilting over

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KMC	Draw De
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☐ 3. Document ID: US 6117725 A

L4: Entry 3 of 4

File: USPT

Sep 12, 2000

US-PAT-NO: 6117725

DOCUMENT-IDENTIFIER: US 6117725 A

TITLE: Method for making cost-effective embedded DRAM structures compatible with logic circuit processing

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KMC	Draw De
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☐ 4. Document ID: US 5702988 A

L4: Entry 4 of 4

File: USPT

Dec 30, 1997

US-PAT-NO: 5702988

DOCUMENT-IDENTIFIER: US 5702988 A

TITLE: Blending integrated circuit technology

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KWC	Draw. De
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☐ 1. Document ID: US 6664195 B2

L11: Entry 1 of 8

File: USPT

Dec 16, 2003

US-PAT-NO: 6664195

DOCUMENT-IDENTIFIER: US 6664195 B2

TITLE: Method for forming damascene metal gate

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KMC	Draw D
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☐ 2. Document ID: US 6583012 B1

L11: Entry 2 of 8

File: USPT

Jun 24, 2003

US-PAT-NO: 6583012

DOCUMENT-IDENTIFIER: US 6583012 B1

TITLE: Semiconductor devices utilizing differently composed metal-based in-laid gate electrodes

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KMC	Draw D
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☐ 3. Document ID: US 6559051 B1

L11: Entry 3 of 8

File: USPT

May 6, 2003

US-PAT-NO: 6559051

DOCUMENT-IDENTIFIER: US 6559051 B1

TITLE: Electroless deposition of dielectric precursor materials for use in in-laid gate MOS transistors

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KMC	Draw D
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☐ 4. Document ID: US 6518113 B1

L11: Entry 4 of 8

File: USPT

Feb 11, 2003

US-PAT-NO: 6518113

DOCUMENT-IDENTIFIER: US 6518113 B1

TITLE: Doping of thin amorphous silicon work function control layers of MOS gate electrodes

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KMC	Draw De
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☐ 5. Document ID: US 6465334 B1

L11: Entry 5 of 8

File: USPT

Oct 15, 2002

US-PAT-NO: 6465334

DOCUMENT-IDENTIFIER: US 6465334 B1

TITLE: Enhanced electroless deposition of dielectric precursor materials for use in in-laid gate MOS transistors

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KMC	Draw De
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☐ 6. Document ID: US 6406956 B1

L11: Entry 6 of 8

File: USPT

Jun 18, 2002

US-PAT-NO: 6406956

DOCUMENT-IDENTIFIER: US 6406956 B1

TITLE: Poly resistor structure for damascene metal gate

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KMC	Draw De
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☐ 7. Document ID: US 6300203 B1

L11: Entry 7 of 8

File: USPT

Oct 9, 2001

US-PAT-NO: 6300203

DOCUMENT-IDENTIFIER: US 6300203 B1

TITLE: Electrolytic deposition of dielectric precursor materials for use in in-laid gate MOS transistors

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KMC	Draw De
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☐ 8. Document ID: US 5960270 A

L11: Entry 8 of 8

File: USPT

Sep 28, 1999

US-PAT-NO: 5960270

DOCUMENT-IDENTIFIER: US 5960270 A

TITLE: Method for forming an MOS transistor having a metallic gate electrode that

is formed after the formation of self-aligned source and drain regions

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KWC	Draw. Doc
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Terms	Documents
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L11: Entry 1 of 8

File: USPT

Dec 16, 2003

DOCUMENT-IDENTIFIER: US 6664195 B2

TITLE: Method for forming damascene metal gate

Abstract Text (1):

The present invention relates to a method of forming a damascene gate electrode of highly integrated MOS transistor capable of easily removing a dummy polysilicon layer. The disclosed comprises the steps of forming a dummy gate insulating layer and a polysilicon layer for a dummy gate on a wafer; forming an interlayer insulating layer on the wafer; polishing the interlayer insulating layer to expose a top surface of the dummy polysilicon layer; and wet etching the exposed dummy polysilicon layer using a spin etching process.

Brief Summary Text (5):

In general, a polysilicon gate electrode and a polycide gate electrode have been used as a gate electrode in sub-0.10 micron devices. However, polysilicon gate are associated with problems such as increases in the effective thickness of the gate insulating layer caused by gate depletion and threshold voltage variations resulting from dopant penetration from p.sup.+ or n.sup.+ polysilicon gate to a substrate and/or variations in dopant distribution. Further, it has proven difficult to produce consistent low-resistance conductors having extremely narrow line widths.

Brief Summary Text (6):

Therefore, metal gate electrodes are being developed as a substitute for the conventional polysilicon gate electrodes. Metal gate electrodes can solve the above-mentioned problems by eliminating the need for dopant in the manufacturing process. Metal gate electrodes, therefore, are able to provide threshold voltages that are symmetric between the NMOS and PMOS regions of a CMOS device by using metals that exhibit a work function located in a mid-band gap of silicon. Such metals include tungsten (W), tungsten nitride (WN), titanium (Ti), titanium nitride (TiN), molybdenum (Mo) and tantalum (Ta).

Brief Summary Text (8):

In order to solve these problems, a method has been proposed for forming a metal gate electrode using a damascene metal gate process. In the damascene metal gate process, a polysilicon gate is formed as a dummy gate and then source/drain regions are formed, thereby completing a transistor. The polysilicon gate is then removed and a metal gate is formed using a damascene process.

Brief Summary Text (10):

Referring to FIG. 1A, a silicon oxide layer and a polysilicon layer are formed on a wafer (10), that is, a silicon substrate in a conventional method of forming polysilicon gate electrode and then, the layers are subjected to a patterning process, thereby forming a dummy gate insulating layer (11) and a dummy gate electrode (12).

Brief Summary Text (11):

Subsequently, source/drain regions (13) are formed by implanting ion impurities and spacers (14) are formed on the sidewalls of the dummy gate insulating layer (11) and the dummy gate electrode (12). Here, the source/drain regions may be formed

using a LDD (Lightly Doped Drain) structure by the following steps. Firstly, a dummy gate electrode (12) is formed and then, source/drain regions are implanted with a low dopant concentration. Sidewall spacers (14) are then formed and the source/drain regions are implanted a high dopant concentration.

Brief Summary Text (12):

Referring to FIG. 1B, an interlayer insulating layer (15) is then formed over the resulting structure. The interlayer insulating layer (15) is then subjected to a chemical mechanical polishing (CMP) process as shown in FIG. 1C to remove a top portion of the interlayer insulating layer and expose the surfaces of dummy gate electrodes (12).

Brief Summary Text (13):

Referring to FIG. 1D, exposed dummy gate electrode (12) and dummy gate insulating layer (11) are selectively etched to expose the substrate (10). The removal of the dummy gate electrode (12) and the dummy gate insulating layer (11) produces a trench (16).

Brief Summary Text (16):

FIGS. 1A to 1D show process steps for selectively removing the polysilicon layer forming dummy gate (12). It is important to prevent damage of sidewall spacers (14) and the interlayer insulating layer (15) during the process of removing the polysilicon layer and it is particularly important to prevent damage to the exposed portion of the silicon substrate (10). Further, all residue from the polysilicon layer must be completely eliminated from the trench (16).

Brief Summary Text (17):

FIGS. 2A and 2B show a conventional method of removing a dummy polysilicon layer for a dummy gate electrode. FIG. 2A shows a conventional method of removing a dummy polysilicon layer using a dry etch process and FIG. 2B shows a method using a wet etch process. In FIG. 2A, the dummy polysilicon layer is etched back and then removed using a plasma etch. FIG. 2B illustrates a method in which the dummy polysilicon layer is removed by a static etch process, that is, by dipping wafers (22) into a wet chemical etch bath (21) for a predetermined time.

Brief Summary Text (22):

Therefore, the present invention has been made in order to solve the above-mentioned problems in the prior art. An object of the present invention is to provide a method for forming a damascene metal gate in which a dummy polysilicon layer is etched rapidly using a spin etch process.

Brief Summary Text (23):

In order to achieve the above object, the method for forming a damascene metal gate according to the present invention is characterized by the steps of: forming a dummy gate insulating layer and a polysilicon layer for a dummy gate on a wafer; forming an interlayer insulating layer on the wafer having the dummy polysilicon layer; polishing the interlayer insulating layer to expose a top of surface of the dummy polysilicon layer; and wet etching the exposed dummy polysilicon layer using a spin etch process.

Detailed Description Text (5):

First, a dummy gate oxide layer (32) and a dummy polysilicon layer (33) are formed on a wafer, i.e., silicon substrate (31) and etched to form a dummy gate. Sidewall spacers (34) and source/drain regions are then formed. Subsequently, an interlayer insulation layer (36) is formed on the surface of the resulting structure. The source/drain regions may be formed in a LDD structure by implanting dopant both before and after the sidewall spacers (34) are formed.

Detailed Description Text (8):

Thereafter, although it is not shown in drawings, the remainder of the dummy gate